UNITED STATES PATENT AND TRADEMARK OFFICE

I, Lydia Johnstone, translator to Siemens Shared Services / Siemens Translation Services, of Hyde House, Oldbury, Bracknell, England declare:

1. That I am a citizen of the United Kingdom of Great Britain and Northern Ireland.

2. That I am well acquainted with the German and English languages.

3. That the attached is, to the best of my knowledge and belief, a true translation into the English language of the accompanying copy of the Amendments to the specification filed with the application for a patent in Germany on 31 July 2003 under the number PCT/DE03/02580 and the official certificate is attached hereto.

4. That I believe that all statements made herein of my own knowledge are true and that all statements made on information and belief are true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the patent application in the United States of America or any patent issuing thereon.

Johnstone

For and on behalf of Siemens Shared Services/
Siemens Translation Services

The 2 day of March, 2005

S4-02P11627

Claims

1. Circuit arrangement for determining the average value of an input signal (s) with

a signal input (1, 14) for receiving the input signal (s) and

a signal output (13) for outputting an output signal (g, Q_1 … Q_{n+m}) indicating the average value of the input signal (s),

a counter (10) or a summing unit being arranged between the signal input (1, 14) and the signal output (13) for averaging, said counter being connected on the input side to a comparator (5),

a switching element (6) being arranged in a feedback loop and activated by the output of the comparator (5) to switch to a first reference signal (Pos_Ref) or a second reference signal (Neg_Ref) as a function of the output of the comparator (5), characterized in that
the summing unit or counter (10) has a reset input (RESET), at which a control signal (CTRL) is present, the control signal (CTRL) and the input signal (s) having the same fundamental frequency and/or the same phase angle and/or a constant phase relationship to each other

2. Circuit arrangement according to Claim 1,
characterized in that
the summing unit or counter (10) is connected on the input side to a sigma-delta modulator (2).

3. Circuit arrangement according to Claim 2, characterized in that the sigma-delta modulator (2) has an adding unit (3) or a subtracting unit, an integrator (4) and a comparator (5) and a feedback loop from the output of the comparator (5) to the input of the adding unit (3) or subtracting unit.

4. Circuit arrangement according to at least one of the preceding Claims, characterized in that the summing unit or counter (10) has a clock input (CLOCK), at which a clock signal (CLK) with a predefined clock frequency is present.

5. Circuit arrangement according to Claim 4, characterized in that the input signal (s) is band-limited and has a predefined limit frequency, the clock frequency being a whole-number multiple of the limit frequency.

6. Circuit arrangement according to one of the preceding Claims, characterized in that the clock signal (CLK) and the control signal (CTRL) have a temporally constant phase relationship to each other.

7. Circuit arrangement according to at least one of the preceding Claims, characterized in that the summing unit or adding unit or counter (10) is connected on the output side to an output register (12).

8. Circuit arrangement according to Claim 7, characterized in that
the output register (12) has a control input (LATCH) to control the receipt of data, the control signal (CTRL) being present at the control input (LATCH).